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[\[PDF\] Minimalist Fault Masking, Detection and Recovery Techniques for ...](#)

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**fault detection** latency. The asynchronous **detection** of Single-Event Latchup ... However, if the **processor** which caused the **error** has also managed to command ...

[www.cs.ucla.edu/~rennels/tr9825dc.pdf](http://www.cs.ucla.edu/~rennels/tr9825dc.pdf) - [Similar pages](#)

[Fault tolerant computer system - Patent 5903717](#)

The invention may be employed to **detect** and to correct **errors** in ... **central processor** units (CPU) operating in parallel "lockstep" and having their outputs ...

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[High level self-checking intelligent I/O controller - Patent 4785453](#)

... are operated in **lockstep** as a dual modular redundant **processor** system. ... If a **fault** is **detected**, two independent bus **error** signals are generated on ...

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[EP969372 Sun european software patent - Bus error handling in a ...](#)

EP969372 Sun microsystems inc (US): Bus **error** handling in a computer system ... between a **processor** and an I/O bus a mechanism for labelling a **fault** status ...

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[EP969373 Sun european software patent - I/o handling for a fault ...](#)

EP969373 Sun microsystems inc (US): I/o handling for a **fault** tolerant ... Similarly, the mutex **processor** 120 can **detect** the likely **error** of the release of a ...

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[\[PDF\] NonStop® Advanced Architecture](#)

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(**processor**) **memory**. **Fault** tolerance for storage data is provided by two. mechanisms: end-to-end checksums for **error**, **detection** and mirrored volumes for ...

[doi.ieeecomputersociety.org/10.1109/DSN.2005.70](http://doi.ieeecomputersociety.org/10.1109/DSN.2005.70) - [Similar pages](#)

[\[PDF\] PowerPC Processor News-April 2001: Index page](#)

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either **processor** could have an **error**. Summary. **Lockstep** designs with PowerPC 740 ... advantage of the MMU found on PowerPC processors to catch the **fault** and ...

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[\[PDF\] 2000-01-1052 Delphi Secured Microcontroller Architecture](#)

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confidence in the first **fault error detection**. ... **processor**, and consumes no system resources until. a **fault** is **detected**. There is a software module that ...

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[\[PDF\] SIFT:](#)

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to **synchronize** their clocks. Each. SIFT. **processor** reads. the value of its ... SIFT, **fault** **detection** is based upon. the **processor**/bus **error** table, an ...

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operate in **lockstep**. The **synchronization** of the processors is guaranteed by the hardware on a per instruction basis. A vahte. eomptted by a **processor** in ...

[dx.doi.org/10.1145/123465.123505](http://dx.doi.org/10.1145/123465.123505)

[\[PDF\]](#) [Low Latency and Cheat-proof Event Ordering for Peer-to-Peer Games](#)

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it still has the same playout latency as **lockstep**. In terms ... bucket **synchronization**, except that unicast is used. While ...

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[\[PDF\]](#) [Efficient barrier \*\*synchronization\*\* mechanism for emulated shared ...](#)

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The idea is that when a **processor** has sent all its messages belonging. to a single superstep on their way,. it. sends a **synchronization** mes- ...

[ieeexplore.ieee.org/iel5/9673/30557/01411139.pdf?arnumber=1411139](http://ieeexplore.ieee.org/iel5/9673/30557/01411139.pdf?arnumber=1411139)

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**processor**, bus, and memory bandwidth suffice for handling multiple concur-. speakers) that transfer data to and ... in “**lockstep**” or that graphics output ...

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in strict **lockstep** fashion. A register channel is provided. with a **synchronization** bit that is used to ensure that a. **processor** reading a channel does so ...

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required to operate in **lockstep**. Special **synchronization**. and high speed communication hardware is provided to. enable high speed **processor** interaction. ...

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clocking whereby all the functional units operate in **lockstep** under the con- ... design techniques without any global **synchronization** signals to control the ...

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[\[PDF\]](#) [Exploiting parallelism on a fine-grained MIMD architecture based ...](#)

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consists of multiple processors that operate in **lockstep** executing instruc- ... This is because

frequent **processor synchronization** can potentially result in ...

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analysis and control flow analysis. Generally, other multiple **processor** systems require explicit **synchronization**

of processes by the user. Dis- ...

[arjournals.annualreviews.org/doi/pdf/10.1146/annurev.cs.04.060190.000305](http://arjournals.annualreviews.org/doi/pdf/10.1146/annurev.cs.04.060190.000305)

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design for this new system is based on a digital signal **processor** (DSP) which ... channel boards in **lockstep** by using matched length onboard transmission ...

[www.iop.org/EJ/article/0967-3334/25/1/041/pn4\\_1\\_041.pdf](http://www.iop.org/EJ/article/0967-3334/25/1/041/pn4_1_041.pdf)

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## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	("5903717").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/24 10:55
L2	17	("5903717").URPN.	USPAT	OR	OFF	2006/03/24 10:56
L3	45	"4785453"	USPAT	OR	OFF	2006/03/24 10:56
L4	14	("4628511"   "4785453"   "4965717"   "5068851"   "5146461"   "5235602"   "5365526"   "5491816"   "5687310"   "5758190"   "5764660"   "5826003"   "6012148").PN. OR ("6256753").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/03/24 11:04
L5	472	714/12	US-PGPUB; USPAT	OR	OFF	2006/03/24 11:04
L6	443	714/34	US-PGPUB; USPAT	OR	OFF	2006/03/24 11:04
S1	2	("5020024").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/16 09:15
S2	2	("5353436").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/08 21:46
S3	2	("5896523").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/09 19:40
S7	1	("0974912").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/08 21:47
S8	236	(714/12).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/13 21:00
S9	170	S8 and (syn\$8 or lock-step or lockstep)	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/13 21:02
S10	73	S8 and (syn\$8 or lock-step or lockstep) and interrupt	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/13 21:23
S11	0	("2005/0229035").URPN.	USPAT	OR	OFF	2006/03/13 21:04

## EAST Search History

S12	51316	(syn\$8 or lock-step or lockstep) and interrupt	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/13 21:23
S13	2436	(syn\$8 or lock-step or lockstep) near4 processor and interrupt	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/13 21:23
S14	1630	(syn\$8 or lock-step or lockstep) near4 processor and interrupt and (fault or error)	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/16 09:52
S15	12496	"fault tolerant"	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/16 09:50
S16	1809	(lock-step or lockstep)	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/16 09:53
S17	96	(lock-step or lockstep) same interrupt\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/16 09:53
S18	56	(lock-step or lockstep) same interrupt\$2 and syn\$6	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/16 09:53
S19	78	(lock-step or lockstep) same interrupt\$2 and syn\$8	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/16 10:17
S20	581	(714/11).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/16 10:18
S21	1706	(714/6).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/16 10:23
S22	260	(714/34).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/16 10:23

## EAST Search History

S23	86	S22 and syn\$8	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/16 10:24
S24	50	S22 and syn\$8 and processors	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/16 14:57
S25	49	S22 and syn\$8 and processors and memory	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/16 10:25
S26	726	(714/43).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/17 10:15
S27	1	("2004/0049715").URPN.	USPAT	OR	OFF	2006/03/16 15:19
S28	163	S26 and syn\$8	USPAT	OR	OFF	2006/03/16 15:19
S29	67	S26 and syn\$8 and interrupt	USPAT	OR	OFF	2006/03/16 15:20
S30	16	("4951283"   "5613074"   "5619728"   "5796938"   "5923673"   "6098120"   "6112316"   "6141757"   "6345370").PN. OR ("6510532").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/03/16 16:12
S31	1058	(710/260).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/16 16:12
S32	294	S31 and syn\$8	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/16 16:13
S33	279	S31 and syn\$8 and interrupt	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/16 16:14
S34	156	S31 and syn\$8 and interrupt and (error or fault)	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/16 16:14
S36	36557	"26" and interrupt and syn\$8	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/17 10:16
S37	726	(714/43).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/17 10:16

## EAST Search History

S38	77	S37 and interrupt and syn\$8	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/17 16:37
S39	726	(714/43).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/20 13:18
S40	73	S39 and interrupt and syn\$8 and (fault or error)	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/17 17:06
S41	92	syn\$8 and (lockstep or lock-step) and (fault or error) and stalling	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/17 17:11
S42	39	syn\$8 and (lockstep or lock-step) and (fault or error) and stalling near4 processor	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/17 17:12
S43	256	syn\$8 and dectect\$4 near4 no (fault or error) and stalling near4 processor	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/17 17:13
S49	2	("20020010880").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/20 11:54
S50	726	(714/43).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT ; IBM_TDB	OR	OFF	2006/03/20 13:19
S51	237	(714/12).CCLS.	US-PGPUB; USPAT	OR	OFF	2006/03/22 15:23
S52	260	(714/34).CCLS.	US-PGPUB; USPAT	OR	OFF	2006/03/22 15:23